In the Claims:

**Claims 1-17 (canceled).**

**Claim 18 (currently amended):** A structure comprising:

a substrate having a top surface for receiving a chip, said chip having at least one device electrode;

a die attach bond pad attached to said top surface of said substrate;

a printed circuit board attached to a bottom surface of said substrate;

at least one signal via in said substrate;

at least one bond pad abutting said at least one signal via, said at least one bond pad providing electrical connection between said at least one device electrode of said chip and said printed circuit board;

a plurality of separate thermally conductive vias in said substrate, each of said plurality of separate thermally conductive vias being coupled to a heat spreader, said heat spreader being directly attached to said bottom surface of said substrate;

a downbond coupling said chip to said die attach bond pad.

**Claim 19 (original):** The structure of claim 18 wherein said chip is a semiconductor chip.

**Claim 20 (original):** The structure of claim 18 wherein said substrate comprises organic material.

**Claim 21 (original):** The structure of claim 20 wherein said organic material is selected from the group consisting of polytetrafluoroethylene material and an FR4 based laminate material.

**Claim 22 (original):** The structure of claim 18 wherein said substrate comprises a ceramic material.

**Claim 23 (previously presented):** The structure of claim 18 wherein said at least one signal via is coupled to said at least one bond pad without utilizing a trace.

**Claim 24 (previously presented):** The structure of claim 23 wherein said at least one signal via runs from said top surface of said substrate to said bottom surface of said substrate.

**Claim 25 (original):** The structure of claim 23 wherein said bond pad is electrically connected to said device electrode by a bonding wire.

**Claim 26 (previously presented):** The structure of claim 18 wherein each of said at least one signal via provides an electrical connection between said device electrode and a land, said land being electrically connected to said printed circuit board.

**Claim 27 (previously presented):** The structure of claim 26 wherein said at least one signal via is coupled to said land.

**Claim 28 (previously presented):** The structure of claim 18 wherein each of said at least one signal via provides an electrical connection between one of said at least one bond pad and a land, wherein said land is electrically connected to said printed circuit board.

**Claim 29 (previously presented):** The structure of claim 28 wherein said each of said at least one signal via is coupled to said land.

**Claim 30 (original):** The structure of claim 28 wherein said bond pad is electrically connected to said device electrode by a bonding wire.

**Claim 31 (original):** The structure of claim 29 wherein said bond pad is electrically connected to said device electrode by a bonding wire.

**Claim 32 (previously presented):** The structure of claim 18 wherein said at least one signal via comprises copper.

**Claim 33 (previously presented):** The structure of claim 18 wherein said at least one signal via comprises a thermally conductive material.

**Claims 34-57 (canceled).**

**Claim 58 (currently amended):** A structure comprising:

a substrate having a top surface and a bottom surface;

a die attach bond pad attached to said top surface of said substrate;

a semiconductor chip attached to said top surface of said substrate, said semiconductor chip having a plurality of device electrodes;

a heat spreader directly attached to said bottom surface of said substrate;

a first plurality of separate thermally conductive vias in said substrate, said first plurality of separate thermally conductive vias providing a connection between said semiconductor chip and said heat spreader;

a plurality of bond pads and a second plurality of signal vias arranged such that each one of said plurality of bond pads abuts a separate one of said second plurality of signal vias;

a downbond coupling said chip to said die attach bond pad.

**Claim 59 (original):** The structure of claim 58 wherein said heat spreader is attached to a printed circuit board.

**Claim 60 (previously presented):** The structure of claim 59 wherein said second plurality of signal vias is located in said substrate to provide connections between said plurality of device electrodes of said semiconductor chip and said printed circuit board.

**Claim 61 (previously presented):** The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide an electrical connection between said semiconductor chip and said heat spreader.

**Claim 62 (previously presented):** The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide a thermal connection between said semiconductor chip and said heat spreader.

**Claim 63 (previously presented):** The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between said plurality of bond pads and said printed circuit board, wherein each of said plurality of bond pads is electrically connected to a respective one of said plurality of device electrodes.

**Claim 64 (previously presented):** The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between each one of said plurality of device electrodes and a respective one of a plurality of lands, said plurality of lands being electrically connected to said printed circuit board.

**Claim 65 (previously presented):** The structure of claim 58 wherein said first plurality of separate thermally conductive vias comprise copper.

**Claim 66 (previously presented):** The structure of claim 60 wherein said second plurality of signal vias comprise copper.